(54) **Resitive crosspoint memory array**

(57) A data storage device (8) includes a resistive cross point array (10) of memory cells (12), each cell including a memory element (50) and electrically conductive hard mask material (52) on the memory element (50). The data storage device (8) may be a Magnetic Random Access Memory ("MRAM") device.

EP 1 271 546 A2

Description

[0001]   The present invention relates to data storage devices. More specifically, the present invention relates to a data storage device including a resistive cross point array of memory cells, and in particular short-tolerant memory cells.

[0002]   A typical Magnetic Random Access Memory ("MRAM") device includes an array of memory cells, word lines extending along rows of the memory cells, and bit lines extending along columns of the memory cells. Each memory cell is located at a cross point of a word line and a bit line.

[0003]   The memory cells may include spin dependent tunneling ("SDT") junctions. The magnetization of an SDT junction assumes one of two stable orientations at any given time. These two stable orientations, parallel and anti-parallel, represent logic values of '0' and '1.' The magnetization orientation, in turn, affects the resistance of the SDT junction. The resistance of the SDT junction is a first value if the magnetization orientation is parallel and a second value if the magnetization orientation is anti-parallel.

[0004]   The logic state of an SDT junction may be read by sensing the resistance state of the SDT junction. However, in some architectural configurations, the memory cells in the array are coupled together through many parallel paths. The resistance seen at one cross point equals the resistance of the memory cell at that cross point in parallel with resistances of memory cells in the other rows and columns. In this regard, the array of memory cells may be characterized as a cross point resistor network.

[0005]   A typical SDT junction has a tunneling barrier that is only a few atoms thick. Controlling the fabrication process to produce such thin barriers for an entire array of memory cells is difficult. It is possible that some of the barriers will be thinner than designed and contain structural defects. If certain SDT junctions have tunneling barriers that are defective or thinner than designed, those SDT junctions might be shorted.

[0006]   If one SDT junction is shorted, the shorted SDT junction will be unusable. In a resistive cross point array that does not use switches or diodes to isolate memory cells from one another, the other memory cells in the same column and row will also be rendered unusable. Thus, a single shorted SDT junction memory cell can cause a column-wide error and a row-wide error.

[0007]   Error code correction could be used to recover data from a complete column or row of unusable memory cells. However, correcting a thousand or more bits in a single column or row is costly, both from a time standpoint and a computational standpoint. Moreover, a typical storage device might have more than one column and row with a shorted SDT junction.

[0008]   There is a need to overcome the problems associated with shorted SDT junctions in resistive cross point memory arrays that do not use isolation devices

such as diodes and transistors.

[0009]   According to one aspect of the present invention, a data storage device includes a resistive cross point array of memory cells. Each memory cell includes a memory element and an electrically conductive hard mask material on the memory element. The hard mask material functions as a resistive element in series with the memory element. If a memory element becomes shorted, the shorted memory element will cause only a randomized bit error. However, the hard mask prevents the shorted memory element from causing column-wide and row-wide errors.

[0010]   Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the present invention.

[0011]   Figure 1 is an illustration of an MRAM device including a memory cell array.

[0012]   Figure 2a is an illustration of three memory cells for the MRAM device.

[0013]   Figure 2b is a diagram of an electrical equivalent of a memory cell shown in Figure 2a.

[0014]   Figures 3a and 3b are illustrations of currents flowing through an electrical equivalent of the memory cell array during read operations on a selected memory cell.

[0015]   Figure 4 is an illustration of a method of fabricating a first level of an MRAM chip.

[0016]   Figures 5a-5c are illustrations of a memory cell during various stages of fabrication.

[0017]   Figure 6 is an illustration of an MRAM chip including multiple levels.

[0018]   As shown in the drawings for purposes of illustration, the present invention is embodied in an MRAM device including a resistive cross point array of memory cells. The MRAM device does not include switches or diodes for isolating memory cells from one another during read operations. Instead, the selected memory cell is isolated by applying an equal potential to selected and certain unselected word and bit lines. Applying the equal potential can prevent parasitic currents from interfering with the read operations.

[0019]   During fabrication of the memory array, a hard mask is deposited on a stack of magnetic memory layers and used to pattern the stack into memory elements. Use of the hard mask reduces edge roughness of the memory elements. Edge roughness of the memory elements causes pinning of domain walls, and irregular nucleation of switching. This irregularity and pinning can cause different memory elements to switch at different fields, increasing the variation in switching field. Reducing the distribution in switching fields (or coercivity) reduces the requirements on half select, and potentially reduces the required switching fields. Improving coercivity distribution reduces switching errors.

[0020]   Using an electrically conductive hard mask provides a dual benefit. Hard mask material remaining

on the memory elements after patterning is not removed. The hard mask material is allowed to remain and function as in-series resistive elements for the memory elements. If a memory element becomes shorted, the shorted memory element will cause a randomized bit error. However, the hard mask material prevents the shorted memory element from causing column-wide and row-wide errors. The randomized bit failure can be corrected by ECC far more quickly and easily than a column-wide or row-wide failure. Thus the memory cells may be made short-tolerant without adding any fabrication steps.

[0021] Reference is now made to Figure 1, which illustrates an MRAM device 8 including an array 10 of memory cells 12. The memory cells 12 are arranged in rows and columns, with the rows extending along an x-direction and the columns extending along a y-direction. Only a relatively small number of memory cells 12 are shown to simplify the description of the device 8. In practice, arrays of any size may be used.

[0022] Traces functioning as word lines 14 extend along the x-direction in a plane on one side of the memory cell array 10. Traces functioning as bit lines 16 extend along the y-direction in a plane on an opposite side of the memory cell array 10. There may be one word line 14 for each row of the array 10 and one bit line 16 for each column of the array 10. Each memory cell 12 is located at a cross point of a corresponding word line 14 and bit line 16.

[0023] The MRAM device 8 also includes a row decode circuit 18. During read operations, the row decode circuit 18 may apply either a constant supply voltage (Vs) or a ground potential to the word lines 14. The constant supply voltage (Vs) may be provided by an external source.

[0024] The MRAM device 8 further includes a read circuit for sensing the resistance of selected memory cells 12 during read operations and a write circuit for orienting the magnetization of selected memory cells 12 during write operations. The read circuit is indicated generally at 20. The write circuit is not shown.

[0025] The read circuit 20 includes a plurality of steering circuits 22 and sense amplifiers 24. Multiple bit lines 16 are connected to each steering circuit 22. Each steering circuit 22 includes a set of switches that may connect each bit line 16 to a source of operating potential or a sense amplifier 24. An output of each sense amplifier 24 is supplied to a data register 30, which, in turn, is coupled to an I/O pad 32.

[0026] During read operations, an equal potential method is applied to the memory cell array 10, and the sense currents flowing through the selected memory cells 12 are sensed. The sense currents indicate the logic states of the selected memory cells 12. The equal potential method prevents parasitic currents from obscuring the sense currents and interfering with the read operations. Different variations of the equal potential method may be used. See, for example, the methods and corresponding hardware implementations in assignee's

U.S. Serial No. 09/564308 filed March 3, 2000.

[0027] Figure 2a shows three memory cells 12 of a column of the array 10. Each memory cell 12 includes a memory element 50 that stores a bit of information as an orientation of a magnetization. The memory elements 50 are not limited to any particular type.

[0028] Each memory cell 12 includes a film 52 of hard mask material on each memory element 50. The film 52 is electrically conductive, having a resistance between about 0.5% and 50% of design resistance of the memory element 50. The film 52 functions as a linear resistive element The film 52 is a remnant of a mask layer, which was used to pattern the elements 50 during device fabrication. These resistive elements are not formed on a silicon substrate. Therefore, they do not take up valuable silicon real estate.

[0029] Films 52 made of diamond-like carbon are preferred. The diamond-like carbon is thermally, electrically and structurally stable, even at temperatures as high as 400°C. Resistivity of the diamond-like carbon can be varied by orders of magnitude, depending upon deposition conditions. The resistivity of the diamond-like carbon can be varied by doping with nitrogen (N). The conductivity can be varied from 0.1 ohm-cm to 10^5 ohm-cm, depending on the deposition conditions. Temperature, power and time all affect the properties, and individual deposition systems will be calibrated for the actual conductivity achieved during specific deposition conditions.

[0030] A mask made of diamond-like carbon produces memory elements 50 having consistent shape and uniformity. Consequently, magnetic switching properties of the memory elements are improved. The diamond-like carbon is a very flat material when deposited, and imparts very little topography to the memory cells 12.

[0031] A further advantage of the films 52 is that the films 52 can be made very thin, on the order of 10-100 nanometers. Resistors that are inherently thicker than diamond-like carbon would decrease the available field for switching.

[0032] Each memory cell 12 further includes a first ohmic contact 54 between its memory element 50 and a word line 14, and a second ohmic contact 56 between its memory element 50 and a bit line 16. The word and bit lines 14 and 16 are typically low resistance conductors made of a metal such as aluminum, copper or gold. The ohmic contacts 54 and 56 provide an interface between the metal lines 14 and 16 and the film 52 and the memory element 50. Although the first and second ohmic contacts 54 and 56 are shown as separate elements 52 and 54, it is understood that these separate elements 54 and 56 may be eliminated and the metal lines 14 and 16 may make direct contact with the films 52 and the memory elements 50.

[0033] The memory cells 12 are shown as being deposited on the bit lines (with the word lines 14 on top). However, the memory cells 12 may be deposited on a word line 14 (with the bit lines 16 on top).

[0034] Referring additionally to Figure 2b, resistance

(B) of the film 52 may be between about 0.5% and 50% of design (i.e., intended) nominal resistance (R) of the memory element 50, that is, $0.005R \leq B \leq 0.5R$). A narrower range would be between about 10% and 50% of nominal resistance (R) of the memory element 50 (that is, $0.1R \leq B \leq 0.5R$). For example, the memory element 50 has a design nominal resistance (R) of 1,000,000 ohms and a delta resistance (ΔR) of 200,000 ohms. Using the narrower range, the film has a resistance (B) between 100,000 ohms and 500,000 ohms. Using the wider range, the film 52 has a resistance (B) between 5,000 ohms and 500,000 ohms. In contrast, the ohmic contacts 54 and 56 each have a resistance (C) of about ten ohms.

[0035] In general, the resistance of the film 52 should be low enough to have a minimal effect on read operations and high enough to have minimal effect on write operations. Thus, the actual resistance should isolate the shorted memory element 50 without degrading the sensing of selected memory cells 12, and without degrading properties of writing to the memory cells 12.

[0036] If a memory element 50 is shorted, the resistance of the memory cell 12 will be about equal to the resistance (B) of the film 52. The advantage of the film 52 during a read operation will now be illustrated in connection with Figures 3a and 3b.

[0037] Figure 3a shows an electrical equivalent of a subset of the memory cell array 10 during a read operation. A selected memory cell is represented by a first resistor 12a, and unselected memory cells are represented by second, third and fourth resistors 12b, 12c and 12d. The second resistor 12b represents half-selected memory cells along the selected bit line, the third resistor 12c represents half-selected memory cells along the selected word line, and the fourth resistor 12d represents the remaining unselected memory cells. If, for example, all of the memory cells 12 have a resistance of about R+B and if the array 10 has n rows and m columns, then the second resistor 12b will have a resistance of about $(R+B)/(n-1)$, the third resistor 12c will have a resistance of about $(R+B)/(m-1)$, and the fourth resistor 12d will have a resistance of about $(R+B)/[(n-1)(m-1)]$.

[0038] The first resistor 12a may be selected by applying an operating potential (Vs) to the crossing bit line and a ground potential to the crossing word line. Consequently, a sense current (I_S) flows through the first resistor 12a.

[0039] To prevent sneak path currents from obscuring the sense current (I_S), an equal operating potential (Vb=Vs) is applied to the unselected bit line. Applying this equal potential (Vb) to the unselected bit line blocks the sneak path currents from flowing through the second and fourth resistors 12b and 12d and diverts to ground a sneak path current (S2) flowing through the third resistor 12c.

[0040] The same operating potential (Vb=Vs) may be applied to the unselected word line instead of the unse-

lected bit line, as shown in Figure 3b. Applying this equal potential (Vb) to the unselected word line blocks the sneak path current from flowing through the second resistor 12b and diverts to ground the sneak path currents (S2 and S3) flowing through the third and fourth resistors 12c and 12d.

[0041] Ideal sense amplifiers 24 apply an equal potential to the selected bit line and the subset of unselected word and bit lines. If, however, the sense amplifiers 24 are not ideal, the potentials are not exactly equal and sneak path currents flow though the array 10 during read operations.

[0042] Consider a read operation on a selected memory cell 12 lying in the same column as a memory cell 12 having a shorted memory element 50. The half-selected memory cell 12 still has a resistance at least equal to the resistance (B) of its film 52. Even if the sense amplifiers 24 are not ideal, the half-selected memory cell 12 with the shorted memory element 50 does not divert a significant amount of sneak path current through the shorted memory element 50 and does not significantly affect the current sensing during read operations. As a result, the half-selected memory cell 12 does not cause row-wide and column-wide failures. Only a single randomized bit error results. The single randomized bit error can be corrected quickly and easily by error code correction.

[0043] The films 52 also increase the reliability of write operations on selected memory cells 12. Without the films 52, large write currents would flow through shorted memory elements 50. Moreover, the write currents would be diverted from the selected memory cell 12 to the shorted memory element 50, thereby reducing write currents and causing incorrect data to be written to the selected memory cells 12 in the same row or column. However, the films 52 have a high enough resistance to prevent large write currents from flowing through the shorted memory elements 50 and allowing sufficient write current to flow through the selected memory cells 12.

[0044] Reference is now made to Figures 4 and 5a-5c, which illustrate the fabrication of a first level of an MRAM device. The fabrication will be described in connection with SDT junctions.

[0045] Row decode circuits, steering circuits, sense amplifiers, registers and other memory device circuits are formed in a silicon substrate (80) Bottom traces are formed on the substrate (82). The traces may be formed by deposition or a demascene process.

[0046] A stack of magnetic memory element layers is deposited (84). The stack 110 for SDT junctions may include first and second seed layers 112 and 114, an antiferromagnetic ("AF") pinning layer 116, a pinned ferromagnetic ("FM") layer 118, an insulating tunnel barrier 120, and a sense FM layer 122 (see Figure 5a). The first seed layer 112 allows the second seed layer 114 to be grown with a (111) crystal structure orientation, and the second seed layer 114 establishes a (111) crystal structure ori-

entation for the AF pinning layer 116. The AF pinning layer 116 provides a large exchange field, which holds the magnetization of the pinned FM layer 118 in one direction. The sense FM layer 122 has a magnetization that is free to rotate in the presence of an applied magnetic field.

[0047]   The insulating tunnel barrier 120 allows quantum mechanical tunneling to occur between the pinned and sense layers 118 and 122. This tunneling phenomenon is electron spin dependent, making the resistance of the SDT junction a function of the relative orientations of the magnetization of the pinned and sense layers 118 and 122.

[0048]   An electrically conductive hard mask having appropriate resistivity is deposited on the stack (86). Resistivity can be controlled by deposition conditions.

[0049]   A bit pattern is defined (88). Conventional photolithography or e-beam lithography may be used. Exposed portions of the mask are removed using, for example, a reactive ion etch with oxygen flow (90)

[0050]   The memory elements 50 are etched (92). An ion or chemical etch may be used. The resulting structure is shown in Figure 5b (the mask material is referenced by numeral 124).

[0051]   The mask material that remains is left on the memory elements (94). Gaps between the memory elements are filled in with an isolation dielectric (96), and top traces are deposited on the mask material and dielectric (98). The resulting first level is shown in Figure 5c (the dielectric is referenced by numeral 126).

[0052]   Referring to Figure 6, additional levels 212 may be added to the MRAM chip 210. Each memory cell level 212 includes an array of memory cells. The memory cell levels 212 may be separated by insulating material (not shown) such as silicon dioxide. Read and write circuits may be fabricated on the substrate 214. The read and write circuits may include additional multiplexers for selecting the levels 212 that are read from and written to.

[0053]   The MRAM device according to the present invention may be used in a variety of applications. For example, the MRAM device may be used for long term data storage in devices such as solid state hard drives and digital cameras.

[0054]   The device is not limited to the specific embodiments described and illustrated above. For instance, the MRAM device has been described in connection with the rows being oriented along the easy axis. However, the rows and columns could be transposed.

[0055]   The resistive cross point array is not limited to an array of magnetic memory cells. Memory elements of the memory cells may be of a phase-change material (resistance of phase-change elements is changed from one state to another by a phase alteration of the phase change material, such as a change from a crystalline state to an amorphous state), anti-fuse elements or polymer memory elements (data is stored as a 'permanent polarization' 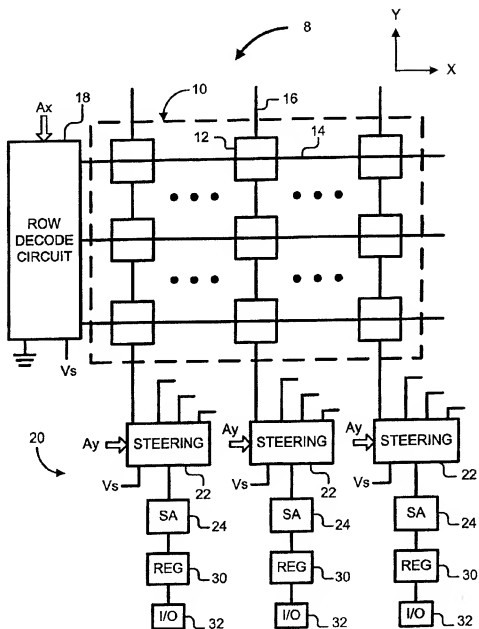in a polymer molecule, and resistance of a polymer memory element is dependant upon the orientation of polarization of the polymer molecules).

[0056]   The present invention is not limited to the specific embodiments described and illustrated above. Instead, the invention is construed according to the claims that follow.
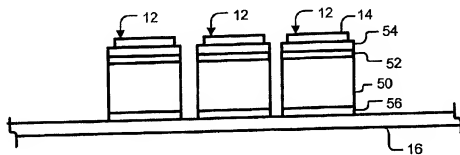
Claims

1. A data storage device (8) comprising a resistive cross point array (10) of memory cells (12), each memory cell (12) including a memory element (50) and electrically conductive hard mask material (52) on the memory element (50).

2. The device of claim 1, wherein the mask material (52) is made of a diamond-like carbon.

3. The device of claim 1, wherein the mask material (52) has a resistance between about 10% and 50% of design resistance of the memory elements (50).

4. The device of claim 1, wherein each memory element (50) includes a spin dependent tunneling junction.

5. The device of claim 1, further comprising:

    a plurality of word lines (14) and bit lines (16) for the array (10); and
    a circuit (20) for sensing resistance states of selected memory cells (12) during read operations on the selected memory cells (12), the circuit applying a first potential to selected bit lines (16), a second potential to selected word lines (14) and a third potential to subsets of unselected word and unselected bit lines (14, 16), the third potential being equal to the first potential.

6. The device of claim 1, further comprising metalization (54, 14) on the mask material (52).
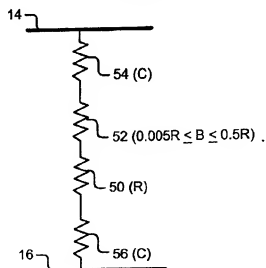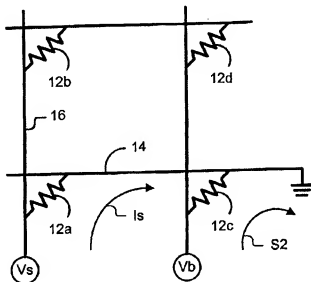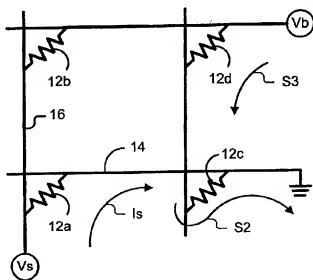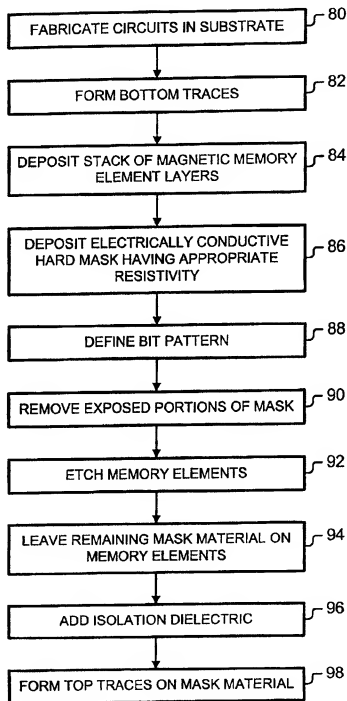
FIG. 1

FIG. 2a

FIG. 2b

FIG. 3a

FIG. 3b

FIG. 4

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┌─────────────────────────────────────┐
│   FABRICATE CIRCUITS IN SUBSTRATE    │ ⌐ 80
└─────────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────────┐
│         FORM BOTTOM TRACES           │ ⌐ 82
└─────────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────────┐
│  DEPOSIT STACK OF MAGNETIC MEMORY    │ ⌐ 84
│          ELEMENT LAYERS              │
└─────────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────────┐
│    DEPOSIT ELECTRICALLY CONDUCTIVE   │ ⌐ 86
│     HARD MASK HAVING APPROPRIATE     │
│             RESISTIVITY              │
└─────────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────────┐
│          DEFINE BIT PATTERN          │ ⌐ 88
└─────────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────────┐
│   REMOVE EXPOSED PORTIONS OF MASK    │ ⌐ 90
└─────────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────────┐
│        ETCH MEMORY ELEMENTS          │ ⌐ 92
└─────────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────────┐
│  LEAVE REMAINING MASK MATERIAL ON    │ ⌐ 94
│          MEMORY ELEMENTS             │
└─────────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────────┐
│       ADD ISOLATION DIELECTRIC       │ ⌐ 96
└─────────────────────────────────────┘
              │
              ▼
┌─────────────────────────────────────┐
│  FORM TOP TRACES ON MASK MATERIAL    │ ⌐ 98
└─────────────────────────────────────┘
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FIG. 5a

FIG. 5b

FIG. 5c

FIG. 6